The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.

What is claimed is:

1. A method of fabricating a rectifier comprising:

epitaxial depositing a semiconductor layer, having a first concentration of a first type of dopant, upon a substrate having a second concentration of said first type of dopant;

etching a plurality of trenches into said epitaxial deposited semiconductor layer;

implanting said epitaxial deposited semiconductor layer proximate a bottom of said plurality of trenches at a third concentration of a second type of dopant, wherein a portion of said epitaxial deposited semiconductor layer proximate walls of said plurality of trenches is not implanted with said second type of dopant, and said implanting forms a plurality of substantially concentric rings of semiconductor material doped with the second type of dopant:

depositing a dielectric in said plurality of trenches; and

depositing a first metal layer upon said epitaxial deposited semiconductor layer, wherein said first metal layer is separated from said epitaxial deposited semiconductor layer implanted with said second type of dopant by said dielectric.

2. The method according to claim **1**, further comprising forming gate definition spacers on said walls of said plurality of trenches prior to said implanting said epitaxial deposited semiconductor layer.

3. The method according to claim **1**, wherein:

said first type of dopant is phosphorous or arsenic; and

said second type of dopant is boron.

4. The method according to claim **3**, wherein:

said first concentration is approximately 5.0E16 to over 1.0E20 cm^3;

said second concentration is approximately 1.0E14 to 5.0E16 cm^{-3}; and

said third concentration is approximately 1.0E 17 to over 1.0E20 cm^{-3}.

5. The method according to claim **1**, further comprising patterning said first metal layer to form a combined anode and anode contact.

6. The method according to claim **1**, further comprising etching said semiconductor substrate to form a plurality of grooves.

7. The method according to claim **6**, further comprising depositing a second conductive layer on said substrate opposite said epitaxial deposited semiconductor layer.

8. The method according to claim **1**, wherein said epitaxial deposited semiconductor layer is approximately 30 nm to 400 nm thick.

9. A method of fabricating a rectifier comprising:

epitaxial depositing a semiconductor layer, having a first concentration of a first type of dopant, upon a substrate having a second concentration of said first type of dopant;

etching a plurality of trenches into said epitaxial deposited semiconductor layer;

forming gate definition spacers on walls of said plurality of trenches prior to said implanting said epitaxial deposited semiconductor layer;

implanting said epitaxial deposited semiconductor layer proximate a bottom of said plurality of trenches and not proximate a portion of each wall of said plurality of trenches, at a third concentration of a second type of dopant, after said forming gate definition spacers, wherein said implanting forms a plurality of substantially concentric rings of semiconductor material doped with the second type of dopant;

filling said plurality of trenches with a dielectric; and

depositing a first metal layer upon said epitaxial deposited semiconductor layer.

10. The method according to claim **9**, wherein:

said first type of dopant is phosphorous or arsenic; and

said second type of dopant is boron.

11. The method according to claim **9**, wherein:

said first type of dopant is boron; and

said second type of dopant is phosphorous or arsenic.

12. The method according to claim **9**, further comprising patterning said first metal layer to form a combined anode and anode contact.

13. The method according to claim **9**, further comprising etching said semiconductor substrate to form a plurality of grooves.

14. The method according to claim **13**, further comprising depositing a second conductive layer on said substrate opposite said epitaxial deposited semiconductor layer.

15. The method according to claim **9**, further comprising annealing said epitaxial deposited semiconductor layer after said implanting, wherein said gate definition spacers limit available diffusion paths during said anneal to shorten a length of a conduction channel formed in said epitaxial deposited semiconductor layer.

16. A method of fabricating a rectifier comprising:

epitaxial depositing a semiconductor layer, having a first concentration of a first type of dopant, upon a substrate having a second concentration of said first type of dopant;

etching a plurality of trenches into said epitaxial deposited semiconductor layer;

implanting said epitaxial deposited semiconductor layer proximate a bottom of said plurality of trenches at a third concentration of a second type of dopant, wherein said implanting forms a plurality of substantially concentric rings of semiconductor material doped with the second type of dopant;

depositing a dielectric in said plurality of trenches; and

depositing a first metal layer upon said epitaxial deposited semiconductor layer, wherein said second type of dopant implanted proximate said bottom of said plurality of trenches is separated from said first metal layer by said dielectric and a portion of said epitaxial deposited semiconductor layer not implanted with said second type of dopant.

17. The method according to claim **16**, further comprising:

forming gate definition spacers on said plurality of walls of said plurality of trenches prior to said implanting said epitaxial deposited semiconductor layer; and

annealing said epitaxial deposited semiconductor layer after said implanting, wherein said gate definition spac-